in said substrate [intersecting] and wherein a well is etched into said substrate through said alternating N-type and P-type layers such that said alternating layer surround said well, said well having a floating gate of conductive material formed therein which is self aligned to not extend laterally beyond edges of said well and insulated from and overlying said alternating N-type and P-type [materials] layers by a layer of gate insulating material;

a word line contact comprising a layer of conductive material formed on said substrate so as to extend down into said well and overlie said [flaotign] floating gate but insulated therefrom by an insulation layer; and

a bit line contact comprising a layer of conductive material formed on said substrate so as to be in electrical contact with the drain region of said vertical MOS transistor formed in said substrate.

2. (Amended) A nonvolatile memory cell array comprised of a plurality of nonvolatile memory cells, each memory cell comprising:

a semiconductor substrate having a drain region of a first conductivity type formed therein and having a surface coincident suitable to act as a drain region of a vertical MOS transistor;

a buried layer channel region in said semiconductor substrate doped so as to have a second conductivity type having the majority of charge carriers therein of a different polarity than said first conductivity type and suitable to act as a channel [region] of a vertical MOS transistor formed in said substrate;

a [first] source region of said semiconductor substrate [between said buried layer and said surface of said substrate, and a second region of said semiconductor

substrate] below said channel region [~~buried layer, both said first and second regions~~].

said source region being doped so as to have [a] said first conductivity type;

[a first layer of insulating material covering said surface of said substrate;]

a recessed gate window in the form of a well etched in said semiconductor substrate through said first layer of insulating material, said well being deep enough to penetrate through said [buried layer] channel region and into said source region such that at least some portion of the side wall or sidewalls of said trench are bordered by said source, drain and channel regions [recessed gate window intersect said buried layer and said first and second regions of said semiconductor substrate];

[a second] an insulating layer covering the bottom of said well;

a gate insulating layer formed on the sidewall of said well;

a self aligned floating gate comprising a conductive material formed within said well on said gate insulating layer so as to not extend beyond the edges of said well; [with]

an insulating layer formed over said self aligned floating gate [conductive material] so as to electrically isolate said floating gate from all surrounding structures, said floating gate having a dimension suitable so as to overlie at least said [intersection of said well with said buried layer] channel region;

a word line comprising conductive material deposited [on said first insulating layer] so as to extend into said well far enough to overlie at least a portion of said floating gate; and

a second layer of insulating material formed [over] so as to insulate at least a portion of said word line; and

a bit line formed over said surface of said semiconductor substrate so as to make contact with at least a portion of said drain region at each said memory cell but insulated

from said word line by said second layer of insulating material[, and deposited in a contact window formed in said first insulating layer so as to be in electrical contact with said first region, said first region acting as a drain of said vertical MOS transitor].

Please add a new claim 3 as follows:

3. A nonvolatile memory cell array comprised of a plurality of EEPROM memory cells, each cell comprising:

a semiconductor substrate;

a vertical MOS transistor formed by a first layer of N-type conductivity and having a surface coincident with the surface of said substrate and forming a drain region of said vertical MOS transistor, a second layer of P-type conductivity within said substrate and adjacent to and underlying said first layer relative to the surface of said substrate and forming a channel region of said vertical MOS transistor, and a third layer of N-type conductivity within said substrate and adjacent to and underlying said second layer and forming a source region of said vertical MOS transistor, and having a well etched into said substrate so as to penetrate through said first and second layers and at least partially through said third layer, said well having a floating gate of conductive material formed therein which is self aligned so as to not extend laterally beyond edges of said well and overlying said first, second and third layers and insulated by a layer of gate insulating material from said first, second and third layers;

a word line comprising a layer of conductive material formed on said substrate so as to extend down into said well and overlie said floating gate but insulated therefrom by an insulation layer;

a bit line comprising a layer of conductive material formed on the surface of said